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TECHNICAL BRIEFS

2014 NOBEL PRIZE IN PHYSICS



Hiroshi Amano

Isamu Akasaki

Shuji Nakamura

The prestigious 2014 Nobel Prize in the Physics was awarded to three former and current members of the IEEE and Electron Devices Society, Isamu Akasaki and Hiroshi Amano and Shuji Nakamura, "for the invention of efficient blue light-emitting diodes which has enabled bright and energy-saving white light sources." The prize, with an award of SEK 8M (£690,000), was shared by the three winners who received their medals at a ceremony in Stockholm on 10 December 2014.

In the 1980s Akasaki and Amano working at Nagoya University and Nakamura independently working at the Nichia Corporation focused on the growth of high quality compound semiconductor gallium nitride (GaN) thin films onto substrates. Both teams used metalorganic vapor phase epitaxy techniques to deposit GaN material which is ideal for blue light emission due to its large band-gap energy corresponding to ultraviolet light. Currently, Akasaki works at Meijo University and Nagoya University, Amano at Nagoya University, Nakamura at University of California, Santa Barbara.

The members of the IEEE Electron Devices Society should be very pleased by the fact that three members of our community were recognized for their device contributions with the 2014 Nobel Prize in Physics. In addition, they have been recognized with numerous awards for their achievements. GaN LEDs are now used in a wide range of applications, from televisions, mobile handheld devices, to street lighting.

Paul Yu
Jr. Past President
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GaN BASED BLUE LIGHT EMITTING DIODES AND LASERS

S. MOKKAPATI AND C. JAGADISH

2014 Nobel Prize in Physics highlights the impact efficient blue light sources have had on our lives. These light sources have penetrated almost every aspect of our lives. The first thing most of us look at when we wake up every day is probably a smart phone screen to check the time. Such displays would not have been possible without small, efficient blue light sources. Blue light emitting diodes (LEDs) are currently used to generate white light for energy efficient lighting applications. Lighting consumes ~20 % of our total electricity consumption. If we make a complete shift to LEDs for lighting applications, we would be reducing our energy consumption significantly. This will result in huge savings with minimal effort.

The journey from the first demonstration of LEDs to the first demonstration of blue LEDs spanned almost 85 years. The device concepts that were used for the initial demonstration of blue light sources were already developed and in fact, were used for demonstration of red/infrared light emitting diodes and lasers in the 1960s. However, it took 30 more years to be able to generate efficient blue light sources. We give a brief history of the developments that lead to the first blue light sources and developments following the first demonstrations. We will discuss the important milestones in the development of blue LEDs/lasers for each of the components below that are essential for any light emitting device:

- Semiconductor layers that efficiently convert electrons into light
- Strategies for electron and light confinement
- Efficient carrier injection and contact layers

ZnSe and SiC were the wide bandgap semiconductors initially

investigated in 1990s for blue light emission. GaN is a direct bandgap (3.4 eV) semiconductor that emits in the ultra-violet region. GaN exists in both cubic and hexagonal lattices. Good quality semiconductors for the active layer of light emitting devices are grown using epitaxial techniques. Lattice matching between the growth substrate and the epitaxial layers to be grown is an important criterion for the growth of high quality semiconductor layers. Lack of a lattice matched substrate for growth of GaN is still a significant issue for epitaxy of GaN and related compounds. Initial efforts on GaN epitaxial growth were based on sapphire substrates. Sapphire substrates are still used for GaN growth even though GaN substrates are available.

Initial growth studies of GaN were based on Hydride Vapour phase epitaxy (HVPE). Development of Molecular beam epitaxy (MBE) and Metal-Organic Chemical Vapour Deposition (MOVPE) in the 1970s proved to be a major milestone in the development of semiconductor light emitting devices. Isamu Akasaki began studies on MOVPE growth of GaN as early as 1974 at Matsushita Research Institute, Tokyo. He continued working on GaN growth with Hiroshi Amano when he moved to Nagoya University in 1981. Akasaki and Amano developed MOVPE for GaN growth on AlN buffer layers on sapphire substrates^{1,2} and Shuji Nakamura at Nichia Chemicals developed the same growth technique for GaN on GaN buffer layers on sapphire substrates³. An optimized buffer layer reduced the interfacial energy between the GaN layers and the substrate and promoted lateral growth.

After successful demonstration of photoluminescence from GaN layers epitaxially grown on AlN or GaN

buffer layers, the next step towards fabrication of electrically injected light emitters in the blue/UV region was to tackle the issue of p-doping. Researchers were able to dope the large bandgap semiconductors with donors (n-type), but acceptor (p-type) doping was still an unresolved issue that inhibited the development of blue light sources. Zn and Mg are used as acceptors for MOVPE growth of semiconductors. p-type behaviour in electron beam irradiated GaN was observed by Akasaki and Amano in late 1980s⁴. Understanding of the phenomenon was later developed by Nakamura who suggested that the acceptors form complexes with hydrogen and become inactive. A heat treatment or electron beam irradiation was necessary to activate the dopants. Successful understanding and demonstration of p-doping in GaN and related compounds, AlGaIn, InGaIn was an important step in the journey of blue/UV light sources. It enabled fabrication of p-n junctions and contact layers for the fabrication of blue/UV light sources.

The first light emitting devices demonstrated were bulk devices. There is no photon confinement or mode confinement in such devices. A device concept that would allow carrier confinement and optical confinement in the active region and enable low threshold, room temperature lasing is the so called double heterojunction structure (Figure 1(a)). It uses a larger bandgap, lower refractive index barrier layers on either side of the active layer. The bandgap difference results in carrier confinement and the refractive index contrast results in optical confinement (Figure 1(b)). The next important conceptual development in the road towards efficient light emitters was that of introducing quantum confinement into the active region. Confinement

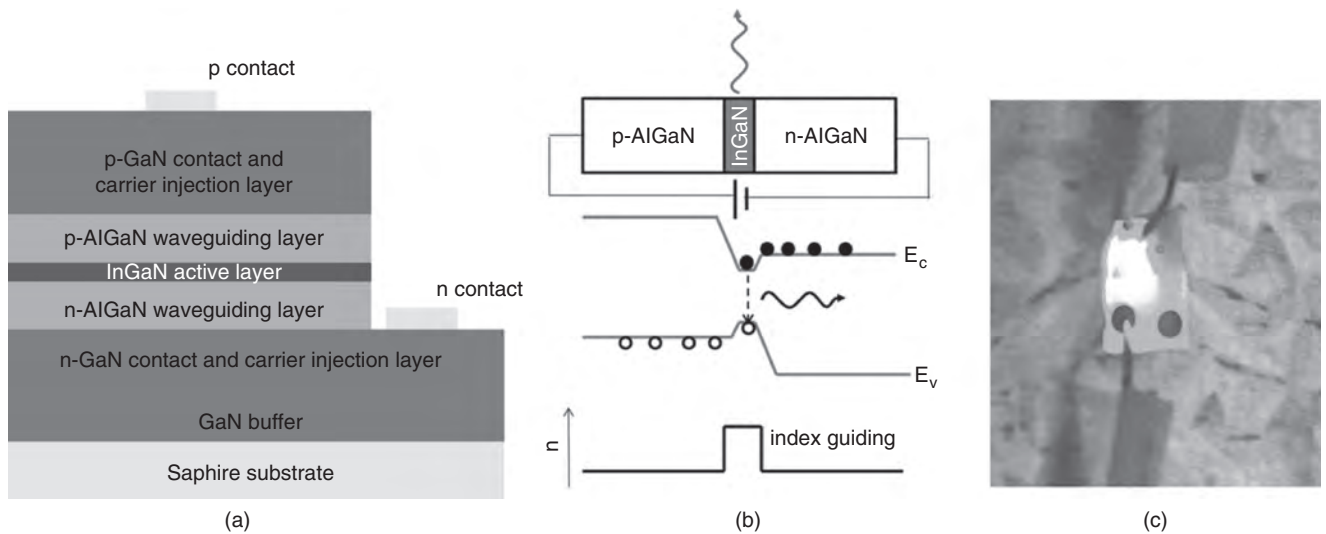


Fig 1. (a) Layer structure of a typical blue double heterostructure. (b) Carrier confinement due to lower bandgap and optical confinement due to higher refractive index in the InGaN region of InGaN/AlGaN double heterostructures. (c) Picture of an actual blue light emitting diode.

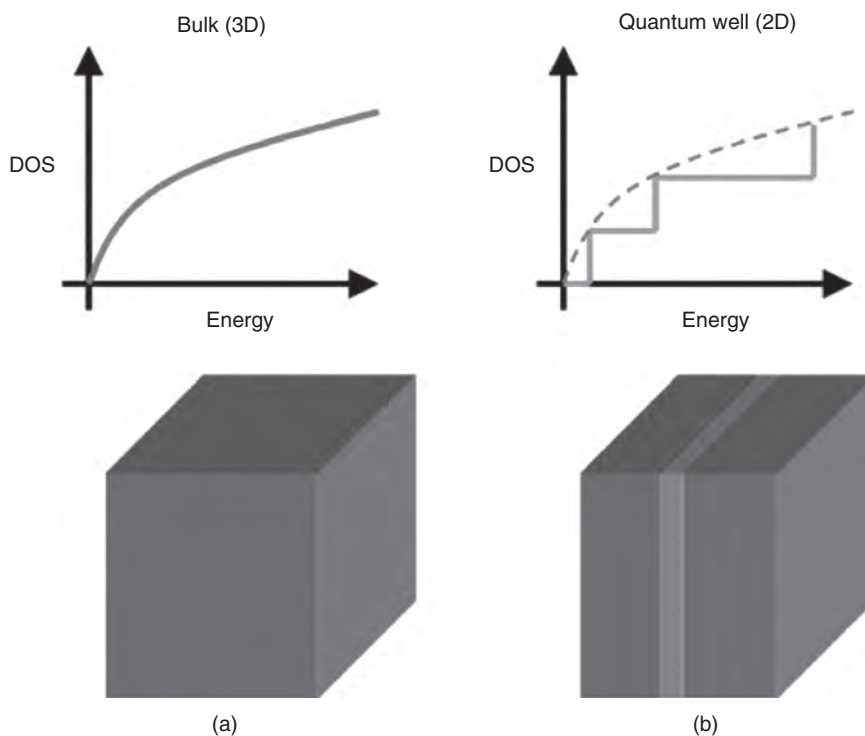


Fig 2. Parabolic density of states in bulk (a) and step function like density of states in a quantum well (b). The step function like density of states in quantum wells results in higher gain at a given carrier injection level resulting in higher output powers for a given input power.

of charge carriers in 1 dimension in what are known as quantum wells modifies the density of states from being a parabolic function of energy in bulk material to a step function in quantum wells (Figure 2). The altered density of states results

in higher gain at any given carrier injection levels compared to bulk material, leading to low threshold, high power devices. Akasaki et. al. investigated AlGaIn/GaN heterostructures while Nakamura et. al. investigated growth of InGaIn quantum wells with

GaN or AlGaIn barriers. They first demonstrated LEDs based on these quantum wells⁵, followed by blue lasers in 1995–96⁶.

AlGaIn/GaN heterostructures are used for emitters in the UV region. The emission wavelength can be relatively blue-shifted by increasing the Al content. Emission below 360 nm is challenging with AlGaIn quantum wells due to increase in the strain in the AlGaIn layers, which results in reduced radiative efficiency. Defect free AlGaIn quantum wells with relatively higher Al content can be grown by using AlN strain reducing interlayers in the GaN buffer (grown on sapphire substrates) and emission in deep UV has been achieved using such structures. Alternatively, InAlGaIn can be used because it is an efficient emitter below 360 nm due to In segregation effects.

InGaIn quantum confined active regions are used for more efficient emission in the blue-green region of the visible spectrum. GaN or AlIn(Ga)N are usually used as barriers for InGaIn quantum well light emitting devices. AlIn(Ga)N cladding layers result in blue-shifted emission with higher intensities from the InGaIn quantum structures due to enhanced quantum confinement. Typical InGaIn quantum well devices

exhibit reduced efficiencies at higher injection currents due to carrier escape from the active region. This is a serious problem with high power lasers that typically operate at high injection densities. Use of AlGaIn/GaN multi quantum well barriers as carrier blocking layers has resulted in improved slope efficiency and reduced threshold currents in InGaIn devices. The AlGaIn/GaN barriers also reduce the effect of strain in the InGaIn quantum well active region compared to quantum well structures capped with AlGaIn. Use of Al containing super lattices in the GaN buffers (grown on sapphire substrates) has also resulted in improved device performance due to strain compensation and reduced threading dislocation density in the devices as Al containing layers act as filters for these dislocations.

Efforts are still ongoing to improve the quality of epitaxial layers used for blue/UV light sources. The crystallographic structure of wurtzite group-III nitrides induces a piezoelectric dipole across the typically c-axis oriented quantum structures in the active region of GaN based devices. The associated electric field leads to a spatial separation of electrons and holes and consequently results in reduced radiative recombination efficiency of the device. The piezoelectric dipole moment associated with the structures increases in magnitude with increasing In content in InGaIn/GaN quantum wells, which is a serious issue for blue-green emitters. The effects of piezoelectric polarization can be eliminated/reduced by growing III-nitride semiconductor structures on non-polar (e.g. a-plane or m-plane GaN or r-plane sapphire) or semipolar (e.g. 1122 GaN) substrates. (AlInGa)N heterostructure devices grown on

non-polar/semipolar directions have been demonstrated and show comparable or better performances than similar devices grown on polar substrates. Improving the efficiency of light extraction from high In content InGaIn/GaN heterostructures seems to be the current focus of research involving GaN based light emitters. Enhanced light emission from long wavelength GaN based emitters has been demonstrated by coupling the quantum structures with surface plasmons or photonic crystal structures.

Current white LEDs rely on converting blue emission using phosphors. This results in inefficient colour rendering for the white LEDs. Colour mixing using red, blue and green LEDs would result in better colour rendering for white LEDs. Lack of efficient green LEDs is the current bottleneck for this application. Current efforts are focussed on realisation of III-nitride based high efficiency green LEDs by investigating novel semiconductor nanostructures like nanowires. Nanowires offer the possibilities of semiconductor growth on lattice-mismatched substrates and light extraction strategies into the active region.

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SYMPTOM OF 'THE END' OF MINIATURIZATION FOR MICRO/NANOELECTRONICS

HIROSHI IWAI

At the beginning of 1970's, the first generation of microprocessors had been introduced with thousands of MOSFETs on a Si chip. This was the beginning of the 'microelectronics' and really the beginning of the technological revolution continuing for half a century. Now entering the 'smart society,' we have to deal with huge amount of information growing every year, and the demand for higher-performance and lower-power-consumption microprocessors becomes stronger and stronger.

The most effective way for realizing the higher-performance and lower-power consumption—per operation—is to miniaturize the MOSFET, because it decreases the capacitance, and hence, results in decrease in the switching time and power consumption of the circuits. The operational voltage reduction accompanied with the miniaturization further decreases the power. That is the reason for the continuous downsizing of the MOSFETs for 45 years until now.

The first generation in early 1970's was that of only p-channel MOSFETs (PMOS LSI) with 10 μm design rule. At that time, even though 'Moore's law' had not been popular at all, and the 'scaling method' had not been published, DRAMs were the technology driver, and many semiconductor companies started to compete each other to decrease the bit cost by increasing the memory capacity at the rate of 4 times per 3 years. Then, the technology finally evolved to CMOS, and 'microelectronics' became 'nanoelectronics,' but still the Si MOS-

FET has been the device used for the circuits. During the period, the technology driver changed to logic LSI's and one generation shrunk to 2 years. The miniaturization has been continued for 19 generations until now as shown in Table 1, and that the area of one MOSFET decreased to quarter million times.

Very few people could predict such a tremendous success in the miniaturization, and there have been many predictions for the limit of the downsizing at 1, 0.5, 0.25 and 0.1 μm , respectively. Very fortunately, new technologies—ion-implantation, dry etching, metal/high-k gate stack, SOI, fin-FET, etc.—, solved the problems, and the predictions turned out not to be true.

What would be the future? Table 2 shows the future predictions of the downsizing by ITRS 2013, published in April 2014. The downsizing will continue for future 7 generations with the shrink rate of 0.7 times every 2 years, and would reach '1.3 nm' in 2027. However, it is only for the 'commercial' name, and real 'physical' parameters such as the metal half pitch and gate length in 2027 are 8 and 5.6 nm, respectively. Thus, the technology in 2027 would be something like that of 8 or 6 nm in reality, and people might be disappointed by the fact. Actually, the shrinking rate for one generation of metal line pitch, gate length (L_g), supply voltage (V_{supply}), equivalent gate oxide thickness (t_{ox}), and Si layer thickness (t_{Si}) for SOI and fin-FET, are expected to be much larger and 0.80, 0.83, 0.96, 0.91 and 0.84, respectively. In fact, the physical

gate lengths of 14 nm technologies are already as large as 25 nm in some semiconductor companies.

There are difficult problems waiting us to limit the downsizing. They are 1) difficulty in EUV lithography development, and cost increase for the double/triple/quadruple lithography as the alternate, 2) increase in the leakage current of MOSFETs, 3) decrease in on-current or drivability of MOSFETs, 4) increase in the capacitance and resistance of the interconnects, 5) degradation in variability, reliability and yield.

Increase in the leakage current of MOSFETs and decrease in on-current or drivability of MOSFETs can be further explained. With downsizing MOSFETs, four leakage current components of the MOSFETs become problematic; i) punch-through between S (source) and D (drain), ii) direct-tunneling between S and D, iii) subthreshold leakage between S and D, and iv) gate oxide leakage between G (gate) and S, C (channel) and D. Punch-through can be suppressed by controlling the channel potential fixed to 0V, by decreasing V_{supply} and t_{ox} , and adopting multi-gate structure (FDSOI-, or fin-FETs) with decreasing t_{Si} . Direct tunneling is believed to be the fundamental limit at the gate length of 3 nm. Subthreshold leakage is suppressed by keeping threshold voltage (V_{th}) as high as possible, but it is difficult as V_{supply} is decreased gradually with the downsizing. In other words, V_{supply} reduction is very difficult because V_{th} cannot be decreased. Gate oxide leakage is fortunately believed not to become the limiting factor until the '1.3 nm generation' in which L_g and t_{ox} are assumed to be 5.6 nm and 0.43 nm (EOT), respectively (see Table 2). We have already confirmed the one order of magnitude

Table 1. Past technology generations for MOSLSIs.

(1970) 10 μm \rightarrow 8 μm \rightarrow 6 μm \rightarrow 4 μm \rightarrow 3 μm \rightarrow 2 μm \rightarrow 1.2 μm \rightarrow
0.8 μm \rightarrow 0.5 μm \rightarrow 0.35 μm \rightarrow 0.25 μm \rightarrow 180 nm \rightarrow 130 nm \rightarrow
90 nm \rightarrow 65 nm \rightarrow 45 nm \rightarrow 32 nm \rightarrow 22 nm \rightarrow 14 nm (2014)

Table 2. Shrink rate of parameters calculated from the data in Table FEP2, ITRS 2013

		Year 2013	Year 2027
Commercial name (nm)	$\times 0.70/2$ years	14 (nm)	1.3 (nm)
Metal half pitch (nm)	$\times 0.80/2$ years	40 (nm)	8 (nm)
L_g (nm)	$\times 0.83/2$ years	20.2 (nm)	5.6 (nm)
V_{dd} (V)	$\times 0.96/2$ years	0.86 (V)	0.65 (V)
EOT (nm)	$\times 0.91/2$ years	0.80 (nm)	0.43 (nm)
T_{Si} (nm)	$\times 0.84/2$ years	7.4 (nm)	2.0 (nm)

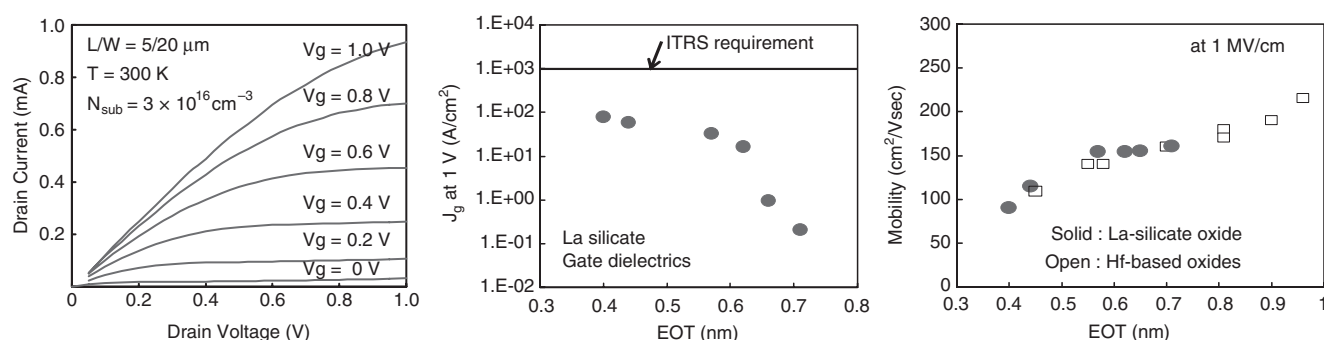


Fig. 1 0.4 nm EOT High-k MOSFET characteristics; (a) I_d - V_d characteristics, (b) gate leakage current vs. EOT, (c) mobility vs. EOT (H. Iwai, Tutorial, ESSDERC 2014).

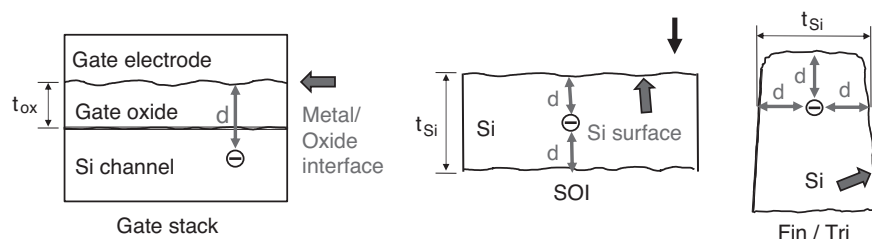


Fig. 2 Interaction between the channel carriers and interface/surface. The interaction becomes stronger as d becomes smaller with decrease in t_{ox} and t_{Si} . (H. Iwai, Tutorial, ESSDERC 2014).

smaller gate leakage current by the experiment of 0.4 nm EOT gate oxide MOSFETs as shown in Fig. 1. Among the 4 components, the sub-threshold leakage current will limit the downsizing, before L_g reaches 3 nm, especially for mobile applications.

Another big problem is the significant decrease in the on-current of MOSFETs with decrease in t_{ox} and t_{Si} . With decrease in these thicknesses, interaction between the carriers and the interface/surface becomes extremely strong as shown in Fig. 2, resulting in the significant decrease in mobility. The reduction of the carrier density under low V_{supply} , due to the

decrease in the density of the state (DOS) when decreasing t_{Si} , is another reason for the on-current reduction.

In conclusion, there is certain high possibility that the downsizing faces its limit in near future because of the increase in the sub-threshold leakage current and lithography process cost, especially in the application of the mobile devices at the gate length of just sub-10 nm. Already its symptom appears in the slowing down of the physical parameter shrinkage rate as shown in Table 2. Recently, there has been a very good challenge in the research of emerging technologies for lower voltage operation, but they are

not yet in the stage for the industry to assume them seriously for next future generations.

However, even though, the downsizing of the MOSFETs will stop in some future, it is not necessary to be too pessimistic. The demand and market size for the microprocessors will keep increasing in future smart society, and thus, the effort to further enhance the performance, and to decrease the power consumption and production cost will be and should be continued even after the 'end of miniaturization.'



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2014 IEEE INTERNATIONAL ELECTRON DEVICES MEETING HIGHLIGHTS

The 60th annual IEEE International Electron Devices Meeting, held in San Francisco from December 15–17, 2014, was attended by some 1,625 of the world's leading scientists, engineers and researchers, who participated in more than 200 technical presentations on the latest developments in advanced semiconductor technology, power devices, novel memory structures, and the medical application of MEMS and other electronic technologies. The conference was preceded by a day of short courses, and a half-day of tutorial sessions.

Among the highlights of the technical program were two late-news papers on 14nm FinFET processes, presented by Intel (employing novel sub-fin doping and air-gapped interconnects on bulk silicon substrates, with ultra-dense SRAM cells for cache memory); and IBM (using a process with 15 levels of copper and embedded DRAM on a silicon-on-insulator substrate). Both presentations, as well as those by TSMC and other chipmakers, indicate that the industry is keeping pace with Moore's Law using FinFET technology.

Power electronics were another highlight of the conference, with the opening plenary talk by Cree's CTO John Palmour detailing progress being made in the area of wide band-gap power devices, specifically third-generation silicon carbide power MOSFETs as well as SiC IGBTs and GTOs ranging from 900V to 27kV, with applications in electric trains and advanced electric grid equipment. In another power talk, NCSU's Dr. Jayant Baliga described the societal impact of advanced power electronic devices—specifically IGBTs—in reducing global electricity consumption by some 50,000 terawatt-hours over the last 25 years.

The expanding medical applications of bio-sensors and MEMS/NEMS



The 2014 IEDM opening plenary talk given by Cree's CTO John Palmour

technology were well-represented, with a paper from the University of Tokyo describing a MEMS tweezer capable of selecting individual DNA molecules for on-chip real-time analysis, which has application in detecting mutated proteins thought to be related to Alzheimer's disease. In another DNA-related paper, Dr. Annette Grot of Pacific Biosciences described the development of high-resolution, high-speed CCD and CMOS image sensors capable of reading optical tags placed on DNA nucleotides, enabling faster and lower-cost DNA sequencing.

Breakthroughs in carbon nanotube array density were presented by researchers from Stanford University, with the first demonstration of highly aligned carbon nanotube FETs with a density of more than 100 CNTs/ μm and drive currents similar to scaled silicon FETs. Their parallel alignment and density was made possible by a new multiple-CNT transfer technique. Another novel manufacturing process was demonstrated by a team from imec, with a programmable 2.1 kHz, 8-bit micro-processor constructed of thin-film transistors inkjet-printed on plastic,

expected to be used in RFID and NFC applications.

Other highlights of IEDM included a Tuesday luncheon address by Cypress Semiconductor CEO/Founder, Dr. T.J. Rodgers, who advocated an alternative view of the causal relationship between CO₂ levels and global temperature patterns, and advised green energy companies to engineer their products to succeed in the marketplace without government subsidies. At the Wednesday Entrepreneurs luncheon, co-sponsored by IEDM & EDS Women in Engineering, Kathryn Kranen, former President/CEO of Jasper Design Automation, shared her advice on establishing a successful startup business in technology. And a special evening panel discussion focused on the past 60 years of innovation at IEDM, and asked the distinguished panel of technology experts to imagine what the next 60 years would reveal.

Next year's IEDM will be held December 7–9, 2015, at the Washington Hilton in Washington, DC. Starting in 2016, the conference will be held in San Francisco, California, each year.

UPCOMING TECHNICAL MEETINGS

2015 IEEE PHOTOVOLTAIC SPECIALISTS CONFERENCE (PVSC)



We invite you to join us for the 42nd IEEE Photovoltaic Specialists Conference (PVSC), being held June 14–19, 2015, in New Orleans, Louisiana. Since our first meeting in 1961, the PVSC has established itself as the world's leading technical event for scientists, engineers and decision-makers across the full spectrum of PV technologies. As PV technologies continue to leap forward at an unprecedented pace, we are expecting yet another tremendous conference.

42nd IEEE PVSC Highlights

Tutorials

The week will begin with a series of educational sessions on PV technologies and markets. These half-day tutorials will offer valuable insights for everyone from industry newcomers who may appreciate the "Photovoltaics 101" sessions, to veterans looking to expand their understanding in new areas, such as Si experts looking to learn how a multi-junction solar cell works. These courses will provide a focused, rapid education in a range of topics of interest to the PV community.

Technical Program

Above all, the PVSC is renowned for its one-of-a-kind technical program, where the world's leading voices in PV present their latest findings and offer forward-looking insights on the future of the industry. For the 42nd meeting, we are expecting over 1,100 submissions, which will bring

you an unparalleled educational experience across 11 topical areas:

Area 1. Fundamentals and New Concepts for Future Technologies

Area 2. Chalcogenide Thin Film Solar Cells

Area 3. III-V and Concentrator Technologies

Area 4. Crystalline Silicon Photovoltaics

Area 5. Thin Film Silicon Based PV Technologies

Area 6. Organic, Perovskite, and Hybrid Solar Cells

Area 7. Space Technologies

Area 8. Characterization Methods

Area 9. PV Modules, Manufacturing, Systems and Applications

Area 10. PV Deployment and Sustainability

Area 11. PV Reliability

Our technology focus spans from the basic technologies through system development and characterization, to deployment. The PVSC is the only PV technology conference that maintains a focus on space technologies in Area 7, which is the birthplace of PV for electric energy generation and continues as the incubator for high efficiency technologies. Areas 9 through 11 form our PV system development and deployment thrust in which we track the transition of PV technologies from development to use in the field and analyze the on-station performance.

The PVSC Exhibit hall will be providing an action-packed floorshow

with an extensive list of companies eager to interface with the PV specialists at the conference. Being the premier technical PV conference, the exhibitors will be those serving the needs of the PV specialist, displaying the latest in solar simulator capability, electrical material characterization, semiconductor growth tools, and many more.

PVSC endeavors to foster as much student participation as possible. We facilitate access to the conference with a reduced student registration rate, and the graduate student assistant program, and we strive to enhance the student's conference experience with events like our student mixer and the best student paper award. We also maintain our PV Jobs portal, which is of keen interest to our students and to our community as a whole.

The IEEE PVSC 42 is shaping up to be our most exciting conference yet, so be on the look-out for our First Call for Papers and mark your calendar for the abstract submission deadline of January 23, 2015 and the conference date of June 14–19, 2015. For more information, visit the conference website: <http://www.ieee-pvsc.org/PVSC42/>.

Robert J. Walters
2015 PVSC Publicity Chair
NRL

Rebekah Feist
2015 PVSC Deputy Publicity Chair
The Dow Chemical Company

2015 IEEE INTERNATIONAL VACUUM ELECTRONICS CONFERENCE (IVEC)



We are very pleased to announce that the Sixteenth International Vacuum Electronics Conference (IVEC2015) will be held April 27–29, 2015, at Beijing International Convention Center (BICC), Beijing, China. Visitors from around the world will experience its long historic, royal architectures and gardens such as the Forbidden City, the Temple of Heaven, the magnificent Ming Tombs, the Summer Palace, the Great Wall, as well as its great changes in the past three decades, particularly the new buildings including the Bird Nest National Stadium and Water Cube Swimming Center for the 2008 Olympic games and also the 2014 APEC Venues which is within walking distance. Beijing is the scientific, educational and cultural heart as well as a key transportation hub which supplies direct flights to most of domestic and international cities.

With technical co-sponsorship from the IEEE Electron Devices Society, the conference will provide a forum for scientists and engineers from all over the globe to present the latest development in vacuum electronics at frequencies ranging from UHF to Terahertz frequency band, as well as their applications.

IVEC was originally created in 2000 by merging the US Power Tubes Conferences and the Europe Space Agency TWTA Workshops. Now a fully international conference, IVEC is held every other year in the US and in Europe and Asia alternately every fourth year. After the successful and enjoyable IVEC2014 in Monterey,

California, IVEC2015 will come to Beijing, China, the first Chinese edition of IVEC after IVEC2003 in Seoul, Korea, IVEC2007 Kitakyushu, Japan and IVEC2011 in Bangalore, India.

IVEC2015 will last three days with one plenary session on the first day and around 30 technical oral and poster sessions planned for the remaining two and half days. Technical presentations spans the range from UHF to THz frequencies, presenting current work in theory and computational tool development, active and passive components, systems, and supporting technologies. Developers of systems will find that IVEC provides a unique snapshot into the current state-of-the-art in vacuum electronic devices. These devices continue to provide unmatched power and performance for advanced electromagnetic systems, particularly in the challenging frequency regimes of millimeter-wave and THz electronics. The meeting is configured to maximally disseminate useful information to device users, manufacturers, academics, and students.

IVEC2015 plenary talks will give the latest progress in the theory and technologies of high frequency and high power vacuum devices, and also provide insights into the broad spectrum of scientific issues and applications that are driving the current directions in vacuum electronics research. There will be a number of topical scientific and commercial applications highlighted, including fusion energy,

medical applications, and RF accelerator technology for high energy physics. From this conference you can have a panorama view of vacuum electronics in Asia, especially China for both education and industry.

The John R. Pierce Award for Excellence in Vacuum Electronics and a Student Paper Award will be presented and as in the past, the meeting and social events will provide unique opportunities to renew or establish new friendships with colleagues, interact with customers, end-users, and meet students and academic researchers.

The conference website is the best source of information about IVEC2015, including Technical Areas, Paper Submission, Registration, Accommodation, and other important dates and events. Please visit <http://cie-china.org/ivec2015> for more details and latest news about the conference. To enquire about exhibitor space and conference support, please contact Dr. Jinjun Feng (fengjj@ieee.org).

You can also learn more about IVEC by visiting the IEEE EDS Vacuum Electronics Technical Committee website: <http://www.vacuumelectronics.org>.

We look forward to seeing you in Beijing.

*Jinjun Feng
2015 IVEC Technical Program Chair
Beijing Vacuum Electronics
Research Institute
Beijing, China*

SOCIETY NEWS

EDS PRESIDENT'S MESSAGE



Albert Wang
EDS President

Dear Fellow

EDS Members,

On September 20, 2014, an EDS ExCom meeting was held at the Universidad Tecnológica de Bolívar, in Cartagena de Indias, Colombia.

Organized concurrently with the Region 9 Chapter Meeting Series, this marks the first EDS ExCom meeting ever held in South America. For more coverage of the R9 Chapter Meeting, see page 29.

Over the past few years, EDS's activities in R9 have been blooming thanks to the great efforts of the local SRC leadership team and, more critically, the EDS members in the region. Outreach programs such as *Engineers Demonstrating Science: an Engineer Teacher Connection (EDS-ETC)*, have been very successful in advancing EDS's mission in Central and South America. Thanks to these efforts, there are now 22 EDS chapters in Region 9! Having the ExCom meeting in Cartagena, Colombia, is a strong endorsement of the Society's activities in Region 9 and I offer special thanks to EDS Secretary Fernando Guarín and the leadership team led by R9 SRC Chair Jacobus Swart.

Many key issues were discussed at the ExCom meeting and action plans were developed accordingly. Bin Zhao, our VP for Publications and Products, provided a detailed analysis of the possible impact the global trend toward open-access (OA) will have on EDS's publication revenue and offered insights on how to best integrate OA into the Society's publication operations. Because publications are a foundational element of what EDS provides its members and the larger technical community, we must do all we can to enhance the quality and accessibility of our technical journals.

Several other items were discussed at the ExCom meeting. I am pleased to announce that you will soon enjoy a new e-Version of the EDS Newsletter. This will not only help transition the Newsletter from the paper format to a fully digital format, but it's far more environmentally friendly.

Regarding Membership and Services, we discussed two options to help make joining EDS more affordable: Society Affiliate membership and the IEEE e-Membership. Promoting affiliate membership will be a key focus going forward. In addition to providing an affordable option for joining EDS, this will help us facilitate collaboration with

other technical societies and organizations. For our members in the developing world, IEEE e-Membership significantly reduces the cost of membership in the IEEE and EDS from about \$200 to \$90.

Leda Lunardi, EDS VP of Technical Committees and Meetings, discussed the action plans to improve technical committee activities, the new technical committee survey, her on-going evaluation of all EDS-sponsored conferences, and the possibility of merging and/or co-locating some of EDS's smaller conferences. With about 80 financially and technically sponsored conferences, it is critical that we frequently review the society's conference portfolio to ensure not only technical coverage of current and emerging trends, but also the fiscal health of our technical meetings.

I will continuously report all EDS activities to you. Meanwhile, it is important that I hear from you, our dear EDS members. So for any ideas, suggestions, and complaints aimed at helping to improve the EDS community, please write to me at eds@ieee.org. The EDS leadership team and I have our ears wide open!

Sincerely,
Albert Wang
from Southern California

MESSAGE FROM EDS VICE PRESIDENT OF TECHNICAL COMMITTEES AND MEETINGS



Leda Lunardi
EDS Vice President
of Technical
Committees and
Meetings

It is my pleasure to write to you as the Vice President of Technical Committees and Meetings, and an elected member of the EDS Board of Governors since January 1, 2014. Having joined IEEE as a student member over 30 years

ago, I have greatly enjoyed the benefits of the EDS network: strong partnerships, loyal friends, and being a part of the global EDS community of dedicated professionals. Among the latter are the members of the technical committees (TCs) which form the core of EDS's conferences, meetings, and publications. Presently there are 14 TCs assembled in areas of EDS interest ranging from conventional topics (such as Semiconductor Devices, Compact Modeling, Device Reliability Physics, Power Devices and Integrated Circuits, VLSI Technology and Cir-

cuits, Semiconductor Manufacturing), through applied areas (TCAD), and multidisciplinary areas (Electronic Materials, MEMS, and Optoelectronic Devices) and more emerging areas (Organic devices, Nanotechnology).

In close partnership with the EDS staff, the leadership of the technical committees and their members have spent a great deal of time in the past year reviewing requests for new or renewed EDS technical sponsorship of meetings and conferences. Presently EDS sponsors over 67 technical meetings. With such a large and diverse conference portfolio, the expertise of the TC members has been essential in reviewing these requests and recommending alternatives addressing meetings and conferences that consistently underperform financially or in terms of attendance.

As a volunteer-driven society we continuously seek and support suggestions from TC members related to new or emerging areas that could be of interest for an EDS-sponsored workshop, mini-symposia or webinar.

This could also include topics for special issues or focused papers for any of the journals and magazines that the society sponsors. For instance, early this year on May 2014 the Optoelectronic Devices Committee Chair TC chair successfully proposed a special issue for the *IEEE Journal of Lightwave Technology* on "Semiconducting Optoelectronic Materials and Devices for Energy Conversion," with publication date planned for November/December of 2015.

As we implement different activities in each respective technical area or when collaborating with other technical societies the **feedback from members like you is vital**. Please let us know your ideas and suggestions, preferably by email to me (leda_lunardi@ncsu.edu) or Ms. Jean Bae, the EDS Senior Conference Administrator (jean.bae@ieee.org).

Sincerely yours,
Leda Lunardi
North Carolina State University
Raleigh, NC, USA

MESSAGE FROM EDITOR-IN CHIEF



M K Radhakrishnan
Editor-in Chief
EDS Newsletter

Dear Readers,
Best Wishes for a Happy New Year 2015. This issue of our Newsletter has many interesting features in contents. Also, we have four new members in our Editorial team, whom I am glad to

introduce.

We have two articles in our Technical Briefs Section, one featuring the latest trends in Silicon Device Scaling and the other on "Blue LED," which elicited in the 2014 Physics Nobel Prize. A short feature on the Nobel Prize winners is

given in the Technical Briefs section. In our Chapter News section, one of our enthusiastic Student Chapter's Vacation Project Mania is featured, which has evaded students from nearby institutions in enjoying the vacation outside and tied down to the campus to enhance engineering innovation. Our Newsletter team would like to hear your views about the contents and suggestions to improve.

Readers' feedback is very important in the growth of our Newsletter. We always like to hear from our members, and the editorial team is looking for constructive criticisms. Please use the e-mail edsnewsletter@ieee.org to convey your ideas and feedback.

Two of our Regional Editors, Fernando Guarín (Regions 1, 2 & 3) and Francisco Sanchez (Region 9) are leaving the team. Fernando being the EDS Secretary and Chairman of EDS Newsletter Oversight Committee is an ardent volunteer guiding and supporting all the developments in the Newsletter and EDS. Francisco has extended the communication between Chapters provided unprecedented exposure to activities of Chapters in Latin America during his tenure as Editor. On behalf of our entire Newsletter team, I would like to express our sincere gratitude to both Fernando and Francisco.

Four new members are joining our Editorial team, out of which

two are women volunteers. Mukta Farooq from IBM will be the Editor for Regions 1, 2 & 3. Joao Antonio Martino of University of Sao Paulo, Brazil is the new Regional Editor for Region 9 – Latin America. In the Region 10 (Australia, New Zealand & South Asia), now we have two Editors in place of my position as Regional Editor. Susthitha Menon from University Kebangsaan Malaysia is the new Regional Editor for Australia and South East Asia in Region 10. Manoj Saxena from University of Delhi is the new Editor for South Asia in Region 10. It is my pleasure to welcome all of them to our team as new Editors of the EDS Newsletter.



Mukta Farooq is an expert metallurgist and materials scientist at the IBM Systems and Technology Group at East Fishkill, New York.

Her areas of expertise include 3 Dimensional silicon integration and packaging, die and wafer stacking for hybrid memory cube and other applications, CMOS FET back end of line structures, flip-chip/C4 technology, lead-free alloys, chip package interaction, and intellectual property.

Mukta is a prolific inventor with over 168 issued U.S. and international patents. She has been designated an IBM Lifetime Master Inventor because of her sustained contributions to intellectual property. She has also authored 25 external publications and has given invited talks at various conferences and universities. Mukta is a founding member of the IBM Semiconductor Technology Symposium held annually, and has served as Technical Chair and General Chair. She is a Senior Member of IEEE, a Distinguished Lecturer of the IEEE EDS, and the Chair of the IEEE EDS Mid-Hudson Valley Chapter.

Mukta is currently a Senior Technical Staff Member at IBM. She has a B.Tech in Metallurgical Engineering

from IIT Bombay, an M.S. in Materials Science from Northwestern University, Evanston, Illinois, and a Ph.D. in Materials Science & Engineering from Rensselaer Polytechnic Institute, Troy, New York.



Joao Antonio Martino is currently a full professor and the head of SOI group at University of Sao Paulo, Brazil. He received masters

(1984) and PhD (1988) degrees in microelectronics from University of Sao Paulo. He was a postdoctoral researcher in silicon-on-insulator (SOI) devices and technology in IMEC, Belgium. His expertise is in electrical characterization, simulation and modeling of SOI devices in wide temperature range. He is also interested in the SOI-CMOS fabrication process, multiple-gate devices (FinFET), 1T-DRAM, Tunnel-FET and radiation effects. He has authored or coauthored of more than 400 technical journal papers and conference presentation and author/editor of 5 books. He is senior member of IEEE and distinguished lecturer of the IEEE Electron Device Society (EDS). He is chair of IEEE ED South Brazil Chapter and vice-chair of Region 9 SRC of IEEE EDS.



P Susthitha Menon is currently an Associate Professor at the Universiti Kebangsaan Malaysia (UKM) at Kuala Lumpur. She received her

BSEE degree from (UKM) in 1998. As an Intel scholar, she worked at Intel Malaysia as a Product Engineer for mobile modules systems from 1999 to 2002. She then received her MSc and PhD (Distinction) degrees in 2005 and 2008 respectively from UKM, for the development of Si- and InGaAs-based interdigitated p-i-n photodiodes. At the University's

Institute of Micro-Engineering & Nanoelectronics (IMEN) she is specializing in the field of optoelectronics, nanophotonics, and robust engineering optimization. Susthitha is a Senior Member of IEEE. She is in the organizing team international conference ICSE by ED Malaysia Chapter for many years and is the Secretary of the IEEE Electron Devices Malaysia Chapter.



Manoj Saxena is an Associate Professor in Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, New Delhi, India.

He received B.Sc. (with honors), M. Sc., and Ph.D. degrees from the University of Delhi in 1998, 2000, and 2006 respectively. He has authored or coauthored 190 technical papers in international journals and various international and national conferences. His current research interests are in the areas of analytical modeling, design, and simulation of Optically controlled MESFET/MOSFET, silicon-on-nothing, insulated-shallow-extension, grooved/concave-gate MOSFETs, cylindrical gate MOSFET and Tunnel FET. He is a reviewer to many journals including Solid State Electronics, Journal of Physics: D Applied Physics and IEEE TED and EDL.

Manoj is a Senior Member of IEEE and also Member of Institute of Physics (UK), Institution of Engineering and Technology (UK), National Academy of Sciences India (NASI) and International Association of Engineers (Hong Kong). Currently, he is the Secretary of EDS Delhi Chapter. For his voluntary contribution, Manoj received the outstanding EDS Volunteer recognition from EDS Chapters in the region in 2012.

*M K Radhakrishnan
Editor-in Chief, EDS Newsletter
e-mail: radhakrishnan@ieee.org*

CALL FOR NOMINATIONS IEEE FELLOW CLASS OF 2016

IEEE Fellow is a distinction reserved for select IEEE members. The honor is conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest.

If you know of an IEEE colleague who is a Senior Member or Life Senior Member in good standing,

has completed five years of service in any grade of IEEE Membership and who has made an outstanding contribution to the electronic or electrical engineering profession in any of the IEEE fields of interest, you can nominate this person in one of four categories: Application Engineer/Practitioner, Educator,

Research Engineer/Scientist or Technical Leader.

Nominations for the Fellow Class of 2016 are now being accepted.

To learn more about the Fellow program and the application process, visit the Fellow Web Site at <http://www.ieee.org/fellows>. The deadline for nominations is 1 March 2015.



Some of the IEEE Fellows who were honored at the 2013 IEDM Plenary.

CONGRATULATIONS TO THE 34 EDS MEMBERS RECENTLY ELECTED TO IEEE SENIOR MEMBER GRADE!

Meng-Fan Chang
Victor Corasaniti
E. Cowell, III
Xiaoli Feng
Wolf Fischer
Akira Fujiwara
Steven Galecki
Nima Ghalichechian
Daniel Green

Fawnizu Azmadi Hussin
John Jackson
Noor Ain Kamsani
Curt Karnstedt
Seongsin Kim
Stephen Kosonocky
Mohdkhairuddin Mdarshad
David Meyer
Ivona Mitrovic

Joel Molina
Martin Mollat
Macaulay Osaisai
Michael Piszczor
Ali Razavieh
Patrick Roblin
Michael Ropp
Suba Subramaniam
Michael Tan

VivekTD
RaviTodi
Akira Toriumi
Reydezel Torres-Torres
Eric Tournie
Zhijian Xie
Woojun Yoon

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US\$25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application: https://www.ieee.org/membership_services/membership/senior/application/index.html.

You will need to Sign-in with your IEEE account.

Please remember to designate the Electron Devices Society as your nominating entity!

2013 EDS GEORGE E. SMITH AWARD

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. The George E. Smith Award was established in 2002 to recognize the best paper appearing in a fast turnaround archival publication of EDS, targeted to *IEEE Electron Device Letters*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The papers winning the 2013 George E. Smith Award were selected from among 480 articles that were published in 2013. The articles are entitled "*Origins of Effective Work Function Roll-Off Behavior for High- κ Last Replacement Metal Gate Stacks*," along with the paper entitled, "*Flexible Complementary Logic Gates Using Inkjet-Printed Polymer Field-Effect Transistors*." These papers appeared in the June 2013 and January 2013 issues of *Electron Device Letters* and were authored by Takashi Ando, Eduard A. Cartier, John Bruley, Kisik Choi, Vijay Narayanan, along with Yong-Young Noh, Kang-Jun Baeg, Dongyoon Khim, Juhwan Kim, Dong-Yu Kim, Si-Woo Sung, and Byung-Do Yang.

The award will be presented at the plenary session of the IEEE International Electron Devices Meeting to be held on December 15, 2014 in San Francisco, California. In addition to the award certificate, the authors will receive a check for \$2,500 to be shared equally among all authors. On behalf of the Electron Devices Society I would like to congratulate the authors for this achievement. Brief biographies of the authors follow.



Takashi Ando received the B.S. and M.E. degrees from the University of Tokyo and the Ph.D. degree from Osaka Uni-

versity in 1999, 2001, and 2010, respectively. He has been a Research Staff Member with the IBM T. J. Watson Research Center, Yorktown Heights, New York, USA, since 2008.



Eduard Cartier earned his Ph.D. from ETH Zurich, did research at ETH and ABB Research in Switzerland. Since 1989 he is RSM at the

IBM T.J. Watson Research in New York, USA, where he works on dielectric degradation and on HK/MG development for advanced CMOS technologies.



John Bruley earned his Ph.D. in Physics from Cambridge University (1988). He held positions at the Max-Planck-Institute for Metals

Research in Stuttgart and the Materials department at Lehigh University. He is currently a senior engineer at IBM's T.J. Watson Research Center. He was recipient of the Microbeam Analysis Society's "Heinrich Award" in 1999.



Kisik Choi is currently a Research Fellow at SK hynix. He contributed to the development of gate stack technologies at IBMT. J. Watson

Research Center in Yorktown Heights, New York, as an assignee of GLOBALFOUNDRIES. Dr. Choi earned BS and MS in Materials Engineering from Seoul National University and a Ph.D. in Electrical Engineering from Texas Tech University.



Vijay Narayanan received the B.Tech. degree in Metallurgical engineering from IIT Madras, India, and the M.S. and Ph.D. degrees in Materials Science and Engineering from Carnegie Mellon University, in 1995, 1996, and 1999, respectively. He joined IBM Research in 2001, where he conducts research on gate-stacks for CMOS Logic. Dr. Narayanan is a fellow of the American Physical Society.



Yong-Young Noh is Associate Professor at Dongguk University in Seoul, South Korea. He received Ph.D. at GIST (2005) and

worked at the Cavendish Laboratory, ETRI, and Hanbat National University. He has received Merck Young Scientist Award (2013) and Korea President Award (2014). His current interest is in printed transistors.



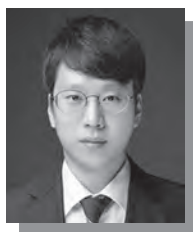
Kang-Jun Baeg is a senior research scientist at Korea Electrotechnology Research Institute. He received his Ph.D. in materials science and engi-

neering from GIST (Korea) in 2010, was a member of engineering staff in ETRI (Korea) from 2010 to 2011, and a post-doctoral research fellow in chemistry at Northwestern University. (in 2012).



Dongyoon Khim received the BS in electronical engineering from Sungkyunkwan University, Korea, in 2008, and the

MS and Ph.D. in material science engineering from the Gwangju Institute of Science and Technology, Korea, in 2009 and 2014, respectively. He has worked at Dongguk University as a postdoctoral research fellow since 2014. His current research interests include the printed electronic devices.



Juhwan Kim received his Ph.D. degree in Materials Science and Engineering from Gwangju Institute of Science and Technology in 2013, and

is currently a postdoctoral researcher at Gwangju Institute of Science and Technology. His research interest is focused on the synthesis of polymers and carbon based materials and their incorporation into electronic devices.

Dong-Yu Kim is Professor of Materials Science and Engineering at Gwangju Institute of Science and Technology,



Republic of Korea. He received Ph.D. at University of Massachusetts Lowell in 1997 and he is a fellow of the Korean Academy of Sci-

ence and Technology. His research interest covers materials and devices for organic electronics, publishing over 200 papers, with H-index above 40.



Si-Woo Sung received B.E. degree in Electronic Engineering and M.S. degree in Semiconductor Engineering from Chungbuk Na-

tional University, Republic of Korea, in 2010 and 2012, respectively. He is an engineer at ADtech, Cheongju, Republic of Korea. His research interests include organic-TFT circuit design and power IC designs.



Byung-Do Yang received the B.S., M.S., and Ph.D. degrees in Electrical Engineering and Computer Science from KAIST, Republic of Ko-

rea, in 1999, 2001, and 2005, respectively. He was a senior engineer at the Memory Division, Samsung Electronics, Kyungki-Do, Republic of Korea, in 2005, where he was involved in the design of DRAM. In 2006, he joined the Department of Electronics Engineering, Chungbuk National University, Republic of Korea, where he is currently an Associate Professor. His research interests are analog circuit, memory circuit, and power IC designs.

Bin Zhao

*EDS Vice President of Publications
Fairchild Semiconductor
Irvine, CA, USA*

2013 EDS PAUL RAPPAPORT AWARD

A high priority of the Electron Devices Society is to recognize and enhance the quality of papers published in EDS archival literature. Every year, the Society confers its prestigious Paul Rappaport Award to the best paper published in the *IEEE Transactions on Electron Devices*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art. The winning paper was selected from close to 600 articles that were published in 2013. The winning paper is entitled, "*High-Mobility Ge p- and n-MOSFETs With 0.7-nm EOT Using HfO₂/Al₂O₃/*

GeOx/Ge Gate Stacks Fabricated by Plasma Postoxidation." This paper was published in the March, 2013 issue of the *IEEE Transactions on Electron Devices*, and was authored by Rui Zhang, Po-Chin Huang, Ju-Chin Lin, Noriyuki Taoka, Mitsuru Takenaka, and Shinichi Takagi.

The award will be presented at the plenary session of the IEEE International Electron Devices Meeting to be held on December 15, 2014, in San Francisco, California. In addition to the award certificate, the authors will receive a check for \$2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the

authors for this achievement. Brief biographies of the authors follow.



Rui Zhang received B.E. and M.E. degrees in materials science and engineering from Tsinghua University, China in 2006 and 2009,

and Ph.D. degree in electrical engineering from University of Tokyo, Japan in 2012. He is currently an assistant professor with Department of Information Science and Electronic Engineering, Zhejiang University, China.



Po-Chin Huang received the Ph.D. degree from the Institute of Microelectronics, National Cheng Kung University, Taiwan in 2012.

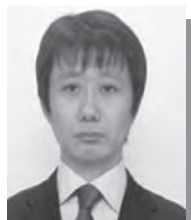
He was a cooperated researcher in the School of Engineering, University of Tokyo, Japan during 2011 to 2012. Currently, he returned to National Cheng Kung University as a postdoctoral research fellow.



Ju-Chin Lin was born in Taichung, Taiwan, on November 8, 1987. She received the B.S. degree in electrophysics from National Chiao

Tung University, Taiwan, in 2011, and the M.S. degree in electrical engineering from the University of Tokyo, Japan, in 2013. She joined

Mitsubishi Electric Corporation, Japan in 2014.



Noriyuki Taoka received Ph.D degree in engineering from Nagoya University, Nagoya, Japan in 2005. From 2005 to 2010, he had

engaged in research of Ge devices in MIRAI project and in the research of III-V & Ge devices at the University of Tokyo, from 2010 to 2011. More recently, in 2012 to 2014, he was involved in the research of IV-IV-alloy systems for electron and optical devices, as an associated professor of Nagoya University. Since 2014, he has been at IHP, Germany, participating in research of IV-IV-alloy systems.

Mitsuru Takenaka received B.E., M.E., and Ph.D. degrees in electronic engineering from the University of Tokyo,



Japan, in 1998, 2000, and 2003, respectively. He is currently an associate professor with the Department of Electrical Engineering and Information Systems, the University of Tokyo.



Shinichi Takagi received the B.S., M.S. and Ph.D. degrees in electronic engineering from the University of Tokyo in 1982, 1984 and 1987, respectively.

He joined the Toshiba R&D Center in 1987. In 2003, he moved to the University of Tokyo as a professor in the School of Engineering.

Bin Zhao
EDS Vice President of Publications
Fairchild Semiconductor
Irvine, CA, USA

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IEEE Foundation





2015 PhD Student Fellowship

Description: One year fellowships awarded to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest. The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

It is expected that three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Middle East/Africa, and Asia & Pacific. Only one candidate can win per educational institution.

Prize: US\$5,000 to the student and if necessary funds are also available to assist in covering travel and accommodation costs for each recipient to attend the EDS Administrative Committee meeting for presentation of the award plaque. The EDS Newsletter will feature articles about the EDS PhD Fellows and their work over the course of the next year.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be pursuing a doctorate degree within the EDS field of interest on a full-time basis; and continue his/her studies at the current institution with the same faculty advisor for twelve months after receipt of award. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electron devices and a proven history of academic excellence.

Nomination Package

- Nomination letter from an EDS member
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date
- One-page biographical sketch of the student (including student's mailing address and email address)
- One copy of the student's under-graduate and graduate transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.
- Two letters of recommendation from individuals familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2015**
- Recipients will be notified by July 15
- Monetary awards will be given by August 15
- Formal award presentation will take place at the EDS Board of Governors Meeting in December

EDS is now accepting nomination package submissions via e-mail, fax and mail!

Email: edsfellowship@ieee.org

Fax: +1-732-235-1626

Mail:

IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:

edsfellowship@ieee.org

Visit the EDS website:

<http://eds.ieee.org/eds-phd-student-fellowship.html>

**May 15, 2015
Submission Deadline**



2015 Masters Student Fellowship

Description: One-year fellowships awarded to promote, recognize, and support graduate Masters level study and research within the Electron Devices Society's field of interest: all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

Three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Mid-East/Africa, Asia & Pacific. Only one candidate can win per educational institution.

Prize: US\$2,000 and a plaque to the student, to be presented by the Dean or Department head of the student's enrolled graduate program.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be accepted into a graduate program or within the first year of study in a graduate program in an EDS field of interest on a full-time basis; and continue his/her studies at a graduate education institution. Nominator must be an IEEE EDS member and preferably be serving as the candidate's mentor or faculty advisor. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform research in the fields of electron devices and proven history of academic excellence in engineering and/or physics as well as involved in undergraduate research and/or supervised project.

Nomination Package

- Nomination letter from an EDS member who served as candidate's mentor or faculty advisor.
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date. This can include undergraduate, graduate and summer internship research work.
- One-page biographical sketch of the student (including mailing address and e-mail address)
- One copy of the student's transcripts/grades
- One letter of recommendation from an individual familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2015**
- Recipients will be notified by July 15
- Monetary awards will be presented by the Dean or Department Chair of the recipient's graduate program at the beginning of the next academic term.

EDS is now accepting nomination package submissions via e-mail, fax and mail!

Email: edsfellowship@ieee.org

Fax: +1 732-235-1626

Mail:

IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:

<http://eds.ieee.org/eds-masters-student-fellowship.html>

**May 15, 2015
Submission Deadline**

YOUNG PROFESSIONALS

EDS-ETC

Engineers Demonstrating Science:
an Engineer Teacher Connection

ED UNIVERSIDAD SANTO TOMAS STUDENT BRANCH CHAPTER, TUNJA, COLOMBIA

EDS student chapter members from Colombia's "Universidad Santo Tomas" in Tunja, Colombia, along with the technical IEEE EDS/RAS chapter participated in the EDS-ETC program working with public schools in the Boyacá region. These schools are under the State's Ministry of Education and are located in the 123 municipalities of the state, some near the capital city of Tunja, but most are distant, rural areas with difficult access conditions.

Through the Ministry of Education's website, word about the EDS-ETC program was sent, getting the message out to all schools. More than 60 schools responded to this call, expressing interest in holding workshops. Due to the remote locations, a training session at the University's Teacher's College in Tunja was held, with students from our EDS chapter providing the training. We currently have 10 Snap Circuits kits, Model SC-100R, and we loaned two kits per school for a period of two weeks. We have developed workshops for a wide range of students from different grades. Workshops have been conducted in over 20 schools in the State of Boyacá, several teachers and about 1,200 students participating in grades starting from sixth grade (ages 9 and 10 years) to juniors (ages 15 and 16 years). We have found wide acceptance and a growing interest from the children and their teachers and a great tool for learning has



Students at the College of Antonio Ricaurte Villa de Leyva with Dr. Guarín.



IEEE Fellows and EDS Distinguished Lecturers, Hiroshi Iwai and Fernando Guarín (center), at Universidad Santo Tomas.

been transformed into a desire to create groups and seed technology research for overcoming the problems of their region.

On the faculty website we have created a page to disseminate the

results of the program and motivate both our students and teachers and college students to participate. The URL is: <http://www.ustatunja.edu.co/ustatunja/index.php/ieee-usta-tunja/programa-eds-etc>.



Fernando Guarin, IEEE Fellow Member, during the video shoot for IEEEtv

For next year we want to continue growing the program, targeting to reach at least 50 more schools,

enhancing our relationship with the Ministry of Education and extending the agreement that was implemented

this year that led to training with kits and robotics to 20 schools. We plan to migrate to working with microcontrollers and complex platforms such as Arduino. With the support of the Electron Devices Society of the IEEE, we will no doubt achieve these and other goals. Last September 13th and 15th we welcomed the visit of IEEE Fellows and Distinguished Lecturers Hiroshi Iwai and Fernando Guarin, who visited Schools in Villa de Leyva and Tunja and also delivered Distinguished Lectures at our University.

*Ricardo Casallas
ED/RA Tunja Chapter Chair
Tunja, Colombia*



IEEE STUDENT TRANSITION & ELEVATION PARTNERSHIP (STEP)

IEEE STEP was developed to provide a dynamic program for facilitating the transition from Student member to young professional by introducing the opportunities and benefits of IEEE membership during the onset of a STEM career.

STEP funding

Funding is available for activities relating to encouraging students to transition to full-member status. This may include holding a graduation reception or seminar on the benefits of IEEE. Events should have a minimum of ten recent graduates and/or soon to graduate IEEE members. Basic funding will be provided at the

amount of US\$500, and additional funding may be available for special circumstances.

Young Professional Section Chairs should submit an application four weeks prior to their scheduled event. Complete the STEP Event Funding Application Form online at, (<https://step.fluidreview.com/>).

In addition, funding will not be granted to an event that has already occurred.

Once the application is submitted, the review process begins with an IEEE volunteer member evaluating the application. All STEP events that go on to be approved and funded by the STEP program budget must

provide the following information within two weeks following the event:

- detailed write-up of STEP event;
- attendance report, minimum ten graduating IEEE members with numbers;
- photos;
- final summary of budget (actual vs. forecast);
- copy of all advertisements used to promote the event (e-mails, invitations, posters, fliers).

Please be sure to take pictures of your event so that others can celebrate with you.

For more information, e-mail the STEP team with questions or comments at step@ieee.org.

IEEE MentorCentre is an online program which facilitates the matching of IEEE members for the purpose of establishing a mentoring partnership. By volunteering as a mentor, members use their career and life experiences to help other IEEE members in their professional development.

PROGRAM BENEFITS AND PRIVILEGES

- Connect with IEEE engineering professionals
- Global community from which to select a mentor
- Career resource offering peer-to-peer guidance
- Included with IEEE membership
- Web-based program providing online practical information for mentoring partnerships

REQUIREMENTS OF BEING AN IEEE MENTOR OR MENTEE

- Giving time and effort to develop a partnership
- Need understanding of role and responsibilities
- Staying in touch and following a plan
- Define goals and outline expectations



**WATCH "IEEE MENTORCENTRE"
ON IEEE.TV, WWW.IEEE.TV.**

Participation in the program is voluntary and open to all IEEE members above the grade of Student Member. For more information on the program, go to www.ieee.org/mentoring. If you have questions, please contact the IEEE MentorCentre Program Coordinator at IEEEmentoring@ieee.org.



"I went to the site and found it easy to navigate, searched by location, and was astounded to have such a wide selection of local potential mentors. I contacted my mentor and arranged a meeting. It is a pleasure to have made such a strong connection, IEEE has honed a valuable service and whether you are a mentor or mentee, there is a great deal or value in this program."

Jamie Garcia
IEEE Member, Mentee

"Helping young engineers develop in their careers is very rewarding. Working with some of these individuals has proven to be quite a challenge, because of the diversity among those seeking mentors. I'm glad to be contributing to this program."

Gary C. Hinkle
IEEE Member, Mentor

JOINING THE IEEE MentorCentre

When you visit the IEEE MentorCentre website, you will be prompted to sign-up as a mentor or mentee. Sign in using your IEEE Web Account. Complete the required fields on you, your work, and interests.

IF YOU ARE A MENTEE begin your search for a mentor.

IF YOU ARE A MENTOR, you will be approved within three business days and then visible in the IEEE MentorCentre system.



THE MATCHING PROCESS

Once you have entered the program, you will complete a user profile form with basic information. Next, the application form requires information to assist in identifying and requesting the search for a match.

The mentees then decide who their ideal mentor will be. Are they looking for someone with their same functional background, or are they interested in a mentor who can help bridge the gap into a new career field? As mentees consider these questions, they will complete their developmental goal setting plan.

FREQUENTLY ASKED QUESTIONS

Q. What is a mentor?

A. A mentor is someone who offers his or her wisdom or experience. A mentor is defined as a wise and trusted counselor or friend. Successful mentors draw from a broad background that is rich with lessons from past experience.

Q. What is a mentee?

A. A mentee has made a commitment of time and energy to engage in a mentoring partnership in hopes of learning from a mentor's "wisdom of experience".

Q. How do I start a mentoring partnership?

A. You will have two forms to complete that capture your basic information, technical interests, educational background and other information about your work. If you are a mentee, you will then search the available mentors in the program to find one you feel match your mentoring needs. Mentors will also be asked to upload their resume or curriculum vitae.

Q. Who selects the mentoring partners?

A. The IEEE mentoring program uses the "informal style" of mentoring, where the mentee self-selects their mentor from a database of available IEEE members who have volunteered to participate. The search criteria is selected by the mentee and can be determined by their geographical preference (country), by technical competencies, societal affiliation, industry, or several other factors.

Q. What kind of commitment should I expect?

A. Each participant in a mentoring partnership should be committed to giving time and effort to develop their partnership. There must be a clear understanding of the roles and responsibilities of each partner and follow an action plan that defines goals and outlines expectations for the partnership. Successful mentoring partnerships should commit to at least two hours per month.

IEEE ResumeLab

Helping IEEE members gain a competitive edge in the employment process.



IEEE ResumeLab is an online service that allows IEEE members to develop a resume or curriculum vitae using specialized tools tailored for each step of the job seeking process.



Resumes/Curriculum Vitae

- Select from a wide array of templates geared toward specific industries, sectors and work experience stages.



Letters

- From cover letter to post-interview thank you letter, ensure optimal communication throughout the hiring process.



Skills Assessment

- Highlight the skills that you possess, your competency in those skills, and what makes your experience with these skills unique.



Mock Interviews

- Prepare for the real thing by selecting an interviewer and the type of questions they'll ask.
- Choose to record your interview for evaluation and feedback.



Video Resumes

- Record custom video messages for potential employers.



Portfolios

- Upload and organize your past work to present to potential employers.



Share Online

- Publish and share everything you create on a publicly viewable website.



Visit IEEE ResumeLab to learn more - www.ieee.org/resumelab



ResumeLab offers something for each phase of a members career:



Student Members

- **Resume module** to put together your first resume for an internship.
- **Portfolio module** to save major projects from your educational experience to share with potential employers.

Young Professional Members

- Prepare for your rounds of interviews by using the **Mock Interview module**. Share the mock interview with a professor or mentor for feedback.
- Don't forget those important cover letters, interview thank you letters, and other critical correspondence. Stand out from the crowd by using the **Letters module** to create great communications.

Mid-Career Members

- Had a resume sitting on a shelf for a while? Get tips on how to refine it by using the **Resume module**.
- Use the **Skills Assessment module** to record your profession specific skills and level of expertise through education and experience.

Prepare for your future employment using IEEE ResumeLab

- Visit www.ieee.org/resumelab.
- Sign in using your IEEE Web Account.
- Create your IEEE ResumeLab profile. The information you enter into IEEE ResumeLab can be different from that used on IEEE.org. To allow better customization of your resume and other resources, it will not be connected to your member record.
- Begin exploring the benefits of IEEE ResumeLab!



ResumeLab is available to IEEE members of any grade at no additional cost. Some features require a computer webcam and high-speed internet connection.

Visit IEEE ResumeLab to learn more - www.ieee.org/resumelab



14-MEMB-236 1/14

Can YOU Change the World?

Show us how and you could win US\$10,000!

The IEEE Presidents' Change the World Competition recognizes students who develop unique solutions to real-world problems using engineering, science, computing and leadership skills to benefit their community or humanity.

Tell us how you have made a positive impact in the world and you could win US\$10,000 plus a free trip to the 2014 IEEE Honors Ceremony.

For complete details and eligibility requirements, visit www.ieee.org/changetheworld

Prizes:



IEEE Student Humanitarian Supreme: US\$10,000

IEEE Distinguished Student Humanitarian: US\$5,000

IEEE Exceptional Student Humanitarian: US\$2,500

IEEE Outstanding Student Humanitarian: US\$1,000
(up to five awarded)

**Submission closes
31 January 2015.**

Follow:  

 **IEEE**
Advancing Technology
for Humanity



IEEE SIGHT

Special Interest Group on Humanitarian Technology



IEEE SIGHT

The Special Interest Group on Humanitarian Technology program serves to promote the mission of IEEE regarding humanitarian technology activities.

Purpose:

Building on the IEEE theme of Advancing Technology for Humanity, the Special Interest Group on Humanitarian Technology will promote activities which use appropriate and sustainable technologies to benefit the vulnerable and underserved sections of humanity.

Application:

Interested in forming a SIGHT group?

Complete the petition and submit the application materials to the SIGHT Steering Committee for review via:

IEEE SIGHT Steering Committee
445 Hoes Lane
Piscataway, NJ 08854-4141
USA

E-mail: h.s.brown@ieee.org
Fax: +1 732 463 3657

For More Information:

Go to <http://bit.ly/11kykcY>

Objectives of SIGHT

- To bring together members / IEEE OUs working in or wishing to work in humanitarian fields and to encourage participation in activities that use humanitarian technologies.
- To increase awareness of IEEE members and engineers of the potential of their work to improve the standard of living of under-privileged populations.
- To engage with NGOs, Civil Society Organizations, UN Organizations, Corporates and other similar bodies in the global engineering community that have common goals to synergize efforts in delivering useful and sustainable technologies in their operations.

Six Easy Steps to Form a SIGHT

- Create a group of six IEEE members. At least three of these signatories must be representatives from two different chapters.
- Affiliate group to an IEEE section or student branch to form a SIGHT Affinity Group (AG).
- Download petition form: <http://bit.ly/16RtF0w>
- Complete the prescribed form and get approval from section chair.
- Send the Petition to SIGHT Steering Committee.
- Receive approval and startup amount from IEEE HQ.

Seed Grants

To help set IEEE SIGHT group activities in motion, the IEEE Humanitarian Ad Hoc Committee will award initial seed grants of US\$250 to each of the first 50 SIGHT groups formed.



QUESTEDS



Samar Saha
EDS President-Elect

Interested in knowing why it's not possible to measure the built-in voltage of a PN junction using a voltmeter? Do you need to understand the best way to derive an expression for the average thermal velocity of an electron? Or are you curious about what quantum dots and wires are? The answers to these questions and more are available through the QuestEDS Question and Answer page.

To ask a question not already addressed on the Q&A page, visit www.ieee.org/go/questeds. Technical experts answering the questions posed represent academic, government, and industry sectors.

Questions are grouped into nine technical categories and two general ones. Technical categories cover subject areas like semiconductor and device physics, process technology, device characterization, technology CAD, compact modeling, VLSI interconnects, photovoltaics, and quantum electronics. Subject areas addressed are anticipated to expand in the future. Two other categories address questions pertaining to educational

Question:

What methodology can be used for quantum approach to transport in nano devices which utilises minimum computation time?

Answer:

The specific method chosen depends on the problem being addressed. Among the many methods for quantum transport, one method has been broadly accepted; the so-called non-equilibrium Green's function (NEGF) method. This method has a firm basis in theory and has been successfully applied to problems from quantum transport in molecules, carbon nanotubes, semiconductor nanowires, nanoscale MOSFETs, spintronic devices, and more. For an introduction to the approach, visit www.nanoHUB.org, search "Datta" and look for the series of four lectures, "Concepts in Quantum Transport."

For simple nanodevices such as carbon nanotubes, the NEGF approach is often quite efficient, but for nanoscale MOSFETs, for example, the computational burden can be very large. (The NEGF approach is equivalent to solving the Boltzmann Transport Equation with one additional dimension.) For nanoscale MOSFETs, the so-called "density-gradient" or "effective potential" approach is often used. This method can be implemented by an added term to the drift-diffusion equation, and it can be used to "include" quantum transport" in Monte Carlo simulation. It is much more efficient than NEGF simulation, but needs to be carefully used and benchmarked against more rigorous methods such as NEGF.

activities and general inquiries about society membership. Within a two week time frame from when the question is asked, an answer is posted online. Incoming questions are handled by an editor-in-chief who ensures that they fall within the technical scope of EDS and that they are adequately answered.

To view the entire library of questions and answers, visit <http://eds.ieee.org/member-sign-in-form.html?notauth=1>. Your IEEE login is required to view the answer page.

Samar Saha
EDS President-Elect
Ultrasolar Technology
Santa Clara, CA, USA

Your PV Connection

IEEE Journal of Photovoltaics

Electronic Version FREE to EDS Members



<http://eds.ieee.org/jpv.html>



CHAPTER NEWS

Region 9 EDS Biannual Chapters Meeting

—by Jacobus Swart and Arturo Escobosa, SRC Region 9 Co-Chairs

On September 20th the EDS Region 9 Chapters Meeting took place in Cartagena Colombia, in the facilities of the Universidad Tecnológica de Bolívar. There were 32 participants, including 6 ExCom members. The meeting was opened by an Overview presented by Jacobus Swart, followed by welcoming remarks by Albert Wang, emphasizing the importance of Region 9 for EDS. Fernando Guarín gave a presentation of EDS Educational Activities. The Chapter presentations were focused on their achievements, activities and problematic since the last meeting. Many of the activities, like talks by distinguished lecturers and mini-colloquia are common to most of the chapters and the majority of chapters participate in local academic events and/or are in close collaboration with the education centers. The snap circuits program, EDS-ETC, has become very popular in the region. In order to introduce children to electronics, some of the actions are targeting to support economically weak communities. Some of the chapters in the region have been created very recently and their members were eager to absorb the experience of the more mature. There are 22 chapters in Region 9 registered with EDS, while 15 of them participated. Some of them could not attend due to logistical difficulties, and some other absences were related to a lack of activities of the chapters. So, most are active chapters.

Three open forum sessions were intercalated to discuss several issues like:

- Interaction between chapters has been the seed of communication between different groups across the region. A proposal to participate in social networks was accepted.



Attendees of the Region 9 EDS Biannual Chapters Meeting.



A representative for the ED/MTT/EMB Brazil Chapter, Luiz Fernando Gadelha (right), accepts on behalf of the chapter, the 2013 EDS Region 9 Chapter of the Year Award. Albert Wang, EDS President (left).

- Alejandro Pérez, Salomão Moraes Da Silva and Jose Cuida volunteered to start a Facebook account.
- Membership is difficult to increase, especially in regular chapters. There are several factors, like lack of semiconductor industry in the area, geographical distance and economic situation, among others. Region 9 individuals can apply for IEEE e-Membership, which is less expensive than the regular fare. An invitation was extended to apply to "Senior Members" to all who qualify.
- An invitation was extended to increase the number of volunteers participating in the EDS Forum activities.
- There are three EDS sponsored conferences in the region, SbMicro, CCE and ICCDCS, and two workshops organized by the IEEE EDS Chapters: SEMINATEC and WAMD.
- All attendees were invited to make an effort to increase the diffusion of their activities in publications like the EDS Newsletter or submitting information for the EDS Region 9 web page (www.edsr9.org)
- The participants were reminded to take advantage of Webinars, Subsidies, Awards: Best Student Paper in Region 9, EDS Chapter of the Year, EDS sponsored conferences.
- It was recommended to include information in the R9 web page such as deadlines for reports and other topics pertinent to the chapters or chapter members as well as links pointing to fellowships, conferences and other pages of interest.

The meeting has shown the region is on track with a solid and active network of chapters.

Region 9 EDS Mini-Colloquium

—by *Jacobus Swart, SRC R9 Chair*
and *Fernando Guarín, Chair of Education Activities*

A mini-colloquium was held at Universidad Tecnológica Bolívar in Cartagena de Indias, Colombia, on September 19, 2014. This mini-colloquium was held in sequence of the biannual EDS Region 9 Chapters Meeting at the same venue. The program was intensive and covered the whole day, with the following series of seven distinguished lectures:

- “Future of Nano CMOS Technology,” by Hiroshi Iwai, Tokyo Institute of Technology, Japan;
- “Field Effect Transistors: From MOSFET to Tunnel FET,” João Antonio Martino, University of São Paulo, Brazil;
- “Operation and Modeling of Junctionless Nanowire Transistors,” Antonio Cedreira, CINVESTAV, Mexico;
- “Operation and Modeling of Junctionless Nanowire Transistors,” Magali Estrada, CINVESTAV, México;
- “Study of Advanced SOI Transistors as Dynamic Memory Cells (1T-DRAM) without the capacitor (Capacitorless),” João A. Martino, University of São Paulo, São Paulo, Brazil;
- “General trends on leading edge semiconductor device fabrication

and future application,” Fernando Guarín, IBM, Fishkill, USA;

- “Young Professionals,” Daniel Camacho, Intel, USA.

This reach program was very much appreciated by the region chapters and participants, bringing valuable information and discussions to the region. After the mini-colloquium a social tour was organized to visit some of the historical sites of Cartagena de Indias.

Vacation Project Mania by ED SJCE Student Chapter, Mysore

—by *C R Venugopal, Chapter Advisor*
ED SJCE

The IEEE ED SJCE Student Chapter organized the Vacation Project Mania 5.0 (VPM), which is one of the signature events of the Chapter. As an annual event aimed at training students to take a head start into working with real time projects where they apply what they have learned, VPM is in its 5th year. VPM saw a massive response this time and many students preferred VPM to start their internships during their vacations. This glorifies the triumph of VPM and instilled a new spirit among the volunteers who made the event a grand success.

VPM is basically a complete training program which makes students think outside the box. From the past

four years, it has earned the reputation of bridging the gap between “What an engineer studies as a part of academics” and “How he has to apply what he has learnt.” VPM is proven to be successful in inducing this drive in the minds of students thus making them industry ready. It is because of this very reason that students decide to stay for VPM leaving their travel plans even during vacations.

The usefulness of last year’s VPM had become so popular in the entire Mysore Hub, that people from all colleges under the hub were eager to take part. So queries were being answered from the past six months for this most awaited event. An entrance test was conducted on April 6, 2014. The test was conducted both in online mode and pen and paper mode so as to aid students from all colleges under the Bangalore Section to take part. There were 256 participants who took the test, out of which only the top 135 students were carefully chosen, including 83 IEEE members

VPM 5.0 was conducted in between June 16th and July 12, 2014. Students were charged as low as Rs.150 for the whole course for IEEE members and Rs.200 for non-IEEE members.

The training mechanism was divided into four phases. The first phase comprised of exposure to projects and the design aspects of analog electronics so as to make students well versed with practical aspects of circuit design, their analysis and trouble shooting. This included both theory and hands on sessions. More fundamentals involving devices and circuits were dealt with. Based on these concepts students were given the task of building systems like burglar alarm and window comparator. Later students voluntarily came up with a number of projects on their own and implemented



Participants of the EDS Region 9 Chapters Meeting held in Cartagena de Indias



Different sessions at VPM organized by the ED Student Chapter, Mysore

them under the guidance of seniors. In the second phase more advanced circuits using microcontrollers, interface modules etc. are learned. Third phase involved software session which became the highlight of this VPM training program. The main objective of this session was to make the students familiar with various software that they could use in their projects to build higher-end applications. Several demo projects involving interfacing hardware and system softwares were displayed. Various softwares like Microsoft Visual Studio, OpenCV libraries, LabVIEW IDE, Matlab, Proteus, Multisim, and open source workbenches like Processing IDE, Arduino IDE, and Energia IDE were introduced. Image processing concepts were discussed and simple projects like color based object tracking, face tracking, multiple object tracking and mouse control using an object Blob in Visual Studio using OpenCV libraries were demonstrated and discussed. They were also introduced to various other microcontrollers like MSP-430, Arduino and also Raspberry pi processor with

their corresponding IDE'S. Finally, the fourth and the most exciting phase of the event was the exhibition of projects developed independently by the participants. IEEE ED SJCE organized this exhibition and competition in the last week of August. All the participants worked on project ideas on any field that they found interesting and submitted their work. The best part of it was that students worked together in teams, shared their ideas, planned and built a project completely on their own. This is the best skill that an IEEE EDS Student Branch could inculcate among the participants. This time the project competition was open for all the colleges in the Bangalore section.

ICSE2014 Conference by ED Malaysia Chapter

—by Burhanuddin Yeop Majlis and P Susthitha Menon

The IEEE Electron Devices Malaysia Chapter organized the 11th IEEE International Conference on Semiconductor Electronics (ICSE2014) at the Berjaya Times Square Hotel, Kuala

Lumpur from August 27-29, 2014. This conference is organized by the ED Malaysia Chapter every two years as a forum for researchers from the world to share their research findings. ICSE2014 had 144 contributed papers for oral and poster presentations in different parallel sessions of Circuits, VLSI & Microwave, Materials & Process, Nanotechnology, MEMS & Microsensors, Materials & Devices and Photonics. More than 150 researchers from 10 different countries attended the conference. The conference was chaired by the IEEE ED Malaysia Chapter Advisor and Founder Director of the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM), Prof. Dato' Dr. Burhanuddin Yeop Majlis.

The first day of the conference had three keynote speakers. Distinguished Prof. Dr. Asad M. Madni from the Electrical Engineering Department, University of California, Los Angeles, USA who delivered a talk entitled "*Convergence of Emerging Technologies to Address the Challenges of the 21st Century*,"



Participants of ICSE2014 at Berjaya Times Square Hotel, Kuala Lumpur

which was followed by Prof. Dr. Edward Yi Chang from the National Chiao Tung University, Taiwan who delivered a speech entitled, *"Realization of GaN-based Technology for Future High Power & High Frequency Applications."* The session ended with a keynote by Prof. Dr. Young June Park from the School of Electrical Engineering, Seoul National University, Korea delivering a speech entitled, *"There is Plenty of Room at the Silicon."*

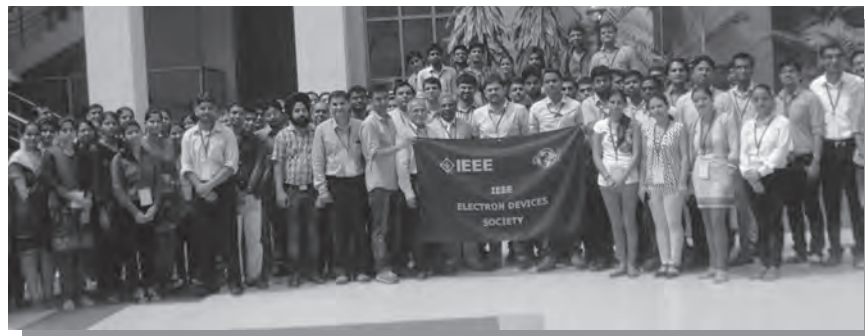
Keynote talks on the second day of the conference started with Prof. Dr. Arokia Nathan from the Electrical Engineering Division, Cambridge University, UK, with his talk entitled, *"Amorphous Oxide Electronics,"* followed by Prof. Dr. Hiroshi Inokawa of Research Institute of Electronics Shizuoka University, Japan with a speech entitled, *"SOI Photodiode with Surface Plasmon Antenna: from Sensitivity Enhancement to Refractive Index Measurement for Biosensing."* The final keynote speaker was Prof. Dr. Abdelkrim Khelif from the French National Centre for Scientific Research (FEMTO-ST), France with his keynote title of *"Acoustic Metamaterials and Phononic Crystals: Towards the Total Control of the Wave Propagation."*

DL-MQ held at IEEE ED Student Chapter, IIT Roorkee —by Pankaj Pal

The IEEE Electron Devices Society (EDS) Student Chapter, IIT Roorkee, organized a mini-colloquium (MQ) on *"Nanoscale Device Physics and Reliability"* on September, 19, 2014. The event was successfully held at the Electronics & Communication Engineering Department of IIT Roorkee. Around 110 participants including Faculty, Research Scholars and graduate students from IIT and various colleges attended this MQ program and there was a good technical interaction among the invited distinguished speakers and the participants. In addition to the talks, there

were two hosted break sessions and a luncheon which provided a venue for fruitful discussions and exchanges of ideas and thoughts. The mini-colloquium featured three IEEE ED Distinguished Lecturers: Dr. Radhakrishnan, NanoRel; Prof. Souvik Mahapatra, IIT Bombay; and Prof. G. N. Dash from Sambalpur University. Dr. Sanjeev Manhas, Chapter Advisor, welcomed the invited speakers and introduced them to the participants. Thereafter, Inauguration was done by lighting the lamp and a speech by Prof. M.V. Kartikeyan, ECE Department HOD of IIT Roorkee. At the start of the technical session, Dr. M. K. Radhakrishnan, EDS BoG Member and Region 10 SRC Vice-Chair, introduced the IEEE ED Society and its various activities and membership benefits to the participants.

The MQ had two sessions with two one and half hour talks each. Dr. Abhishek Dixit from IIT Delhi spoke on *"Designing CMOS Devices and Circuits using Calibrated Models"* and followed by Prof. Souvik Mahapatra from IIT Bombay who gave the DL, *"Bias Temperature Instability in HKMG MOSFETs, Characterization, Process Dependence, DC/AC Modeling and stochastic Effects"*. After lunch, Prof. M. K. Radhakrishnan, NanoRel, gave a DL on *"Silicon Nanodevices-Analysis Challenges and Interface physics."* The final DL was given by Prof. G. N. Dash of Sambalpur University on *"Graphene for Electron Devices."* The MQ was another successful event of the EDS IIT Roorkee Student Chapter.



EDS Distinguished Lecturers and attendees at the IEEE ED MQ, held September 19, 2014, at IIT Roorkee

REGIONAL NEWS

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

ED Dublin/PHO Ireland

—by Patrick McNally

The joint chapter of the Dublin Electron Devices and the Ireland Photonics Societies hosted Professor Brian Tanner in the Rince Institute of Dublin City University during the summer. An audience of over fifty attendees heard Professor Tanner, Dean for University Enterprise and Professor of Physics at Durham University, UK, present a lecture entitled “*University Intellectual Property: What is it Worth?*” Professor Tanner addressed the spectacular rise and fall in the number of UK University start-ups over the past 20 years and discussed the merits of different models of commercialisation of research, in particular how these models would apply in Ireland.

Brian Tanner has been a member of two teams that have spun-out companies based on intellectual property partly generated from his own research, both of which have floated. He is a non-executive

Director of the Kromek Group plc and holds the Queen’s Award for Enterprise Promotion. The large audience included practising engineers and commercialisation specialists, who took part in a lively and stimulating discussion that continued for 45 minutes after the talk.

ED Scotland

—by Anthony Walton

To commemorate the fifth IEEE Day, the Scottish Chapter of EDS held *An Evening’s Exploration of Past, Present and Future Electronics* at the end of September 2014. At the event, over fifty attendees heard talks from two internationally recognized speakers from the field of Electronic Engineering. The first entitled *Words, Wires and Waves: A History of Communication* was given by Prof. Tom Stevenson, formerly the Operations Director of the Microfabrication cleanroom facilities at the University of Edinburgh. Now retired, Tom is the Chairman of the Museum of Communication in Fife, Scotland (www.mocft.co.uk). The second talk, entitled *Every Photon Counts: Single Photon Avalanche Diodes and their Applications*, was given by Dr. Robert Henderson, who



The Evening’s Speakers: Prof Tom Stevenson (left) and Dr Robert Henderson (right)

as principal VLSI engineer in ST Microelectronics Imaging Division led the design of the first image sensors for mobile phones. He joined the University of Edinburgh in 2005 to pursue his research interests in CMOS integrated circuit design, imaging and biosensors.

The talks were followed by a drinks reception in the University of Edinburgh’s Appleton Tower Concourse where a number of table top displays had been set up for guests. Prof Stevenson had brought a range of interactive exhibits from the Museum of Communication’s extensive archives and Dr. Henderson’s research group were running real time experiments demonstrating time correlated single photon counting and time-of-flight 3D imaging. Crowds formed at all the displays and the discussions went on long after the official closing time of the event.

~Jonathan Terry, Editor

ASIA & PACIFIC (REGION 10)

EDS Distinguished Lecture at ED Japan Chapter

—by K. Kakushima

The Iwai Laboratory at Tokyo Institute of Technology hosted a day long visit from Prof. M. Jamal Deen, McMaster



Professor Brian Tanner of Durham University speaking at the Rince Institute in Dublin, Ireland



EDS Distinguished Lecture by M. Jamal Deen, McMaster University, Canada, on July 16, 2014

University, Canada, on July 16, 2014. Dr. Deen is a professor of Electrical and Computer Engineering, and Bio-medical Engineering and holder of the Senior Canada Research Chair in Information Technology, McMaster University. His research interests span a wide range from nanoelectronics, optoelectronics, nanotechnology and their emerging applications to health and environmental sciences. During his visit to Iwai Labs, Prof. Deen gave a presentation on importance on water and introduced new concepts on microtechnology-based sensors for rapid and accurate evaluation of water quality. Also to encourage collaborative research, a tour of Iwai Lab along with a presentation of ongoing research themes in Iwai Lab, was presented to Prof. Deen by some of the Iwai Lab students.

ED Japan

—by K. Kakushima

The ED Japan Chapter held its' annual IRPS Report Meeting at Shibaura Institute of Technology, Tokyo, on

October 3rd. The meeting began with Prof. K. Eriguchi, Kyoto University, briefly introducing the management of the IRPS and Dr. S. Shuto, Toshiba, gave a general review of the conference, which was held in June 2014, followed by topic reviews given by:

- Dr. H. Miki, Hitachi: on process integration and gate dielectrics;
- Dr. H. Matsuyama, Fujitsu Semiconductor: on interconnects;
- Dr. S. Kudo, Renesas: on failure analysis;
- Dr. S. Fujii, Toshiba: on memory reliability;
- Dr. T. Uemura, Fujitsu Semiconductor: on soft-error.

Following the topic reviews, six selected papers from the IPRS were presented by their authors: Prof. K. Lee, Prof. R. Kuroda, Dr. T. Obara (all from Tohoku University); Dr. T. Kikuchi, Toshiba; Dr. N. Suzumura, Renesas; and Prof. S. Yokogawa, Polytechnic University. More than 60 attendees from the academic and corporate communities enjoyed the discussions on the latest material/process/device/circuit reliability.

ED Kansai

—by Michinori Nishihara

The ED Kansai Chapter held a Technical Meeting on October 3, 2014, at OIT



Prof. Taiichi Otsuji



Dr. Takashi Nakamura



Japan Chapter's annual IRPS Report Meeting



Attendees of the Kansai Chapter meeting

UMEKITA Knowledge Center, Osaka, Japan, which attracted 42 attendees by inviting two prestigious lecturers. The first speaker was Prof. Taiichi Otsuji of Tohoku University and the title of his lecture was “*Research Forefront of Graphene Plasmonics for Terahertz Devices*.” Prof. Otsuji began his lecture by explaining the need of terahertz devices for sensing and communication technology and then introduced graphene devices as one of next generation devices to realize terahertz applications possible. He talked about the basic property of graphene, then discussed the most recent research topics in graphene plasmonics including his own contributions, which seemed very promising.

The second lecturer was Dr. Takashi Nakamura of ROHM Co., Ltd. and the title of his lecture was “*Status of Development and Commercialization of SiC Power Devices and Modules*.” SiC power device is believed to be the next candidate of high voltage/power devices to overcome the

limitation of silicon based power devices. He explained the status of SiC power devices in real applications such as voltage converters along the power line and inverters in hybrid electric vehicles. SiC power devices are already penetrating in various applications which require small form factor and light weight.

The next event by the chapter will be to host the IEDM2014 feedback meeting in January 2015. Please check our chapter homepage for more detail: <http://www.ieee-jp.org/japan/council/chapter/ED-15/index.html>.

~Kuniyuki Kakushima, Editor

ED Chapter, Calcutta

–by Soumya Pandit and Swapnadip De

The IEEE EDS Calcutta Chapter co-sponsored the International conference on “Microelectronics, Circuits and Systems,” Micro-2014, organized by IASTM, IETE and PIET Odisha at Hotel Hyatt Regency on July 11,

2014. At the opening session, Shri R.N. Lahiri of IETE Kolkata, mentioned about the current status of CMOS transistors and optoelectronic devices for various applications including logic, memory and power applications. The key note speech was delivered by Prof. Soumya Pandit, Chair, ED Calcutta Chapter, in the domain of Nano-scale Challenges of CMOS Circuits. He elaborated the various deep-submicron issues of MOS transistors and the dominant effects of these on the circuit performances. More than 100 participants, including Professors, Scientists and professionals in the field of electronics, attended the conference. From among the 180 papers received, after peer review, 60 were accepted and presented. The overwhelming response received from authors was really significant. The conference aimed to promote research collaborations among the researchers at local institutions and overseas in a more diversified manner in the new areas of research in Microelectronics, Circuits and Systems and to carry out joint research by bridging of collaborations between universities and industries.

ED Chapter Kuala Lumpur, Malaysia

–by P Sushitha Menon

The IEEE ED Malaysia Chapter organized three Distinguished Lecture (DL) events on August 25, 26 and 29, 2014, at two different locations in Malaysia. On August 25th, Prof. Dr. Edward Chang from the



Speakers and delegates at the Micro-2014 conference organized by ED Calcutta Chapter



Prof Edward Chang with attendees of the DL at UPM, Kuala Lumpur, Malaysia



Prof Arokia Nathan and attendees of DL at UPM Malaysia

National Chiao Tung University, Taiwan R.O.C delivered a DL on *"III-V device for communication and terahertz imaging application,"* at the Faculty of Engineering, Universiti Putra Malaysia (UPM). On August 26th, Prof. Dr. Edward gave another DL entitled *"InAs HEMT for TeraHertz Imaging: Next*

generation Communication and Post CMOS Applications," at the Faculty of Engineering, Multimedia University (MMU) Malaysia. Both talks were attended by more than 80 participants each at both locations.

Dr. Arokia Nathan from the Electrical Engineering Division, Cambridge

University, UK, gave a Distinguished Lecture at the Faculty of Engineering, Universiti Putra Malaysia (UPM) on August, 29, 2014. The talk entitled *"Flexible Electronics,"* was attended by researchers and graduate students from both UPM and MMU, which had a very lively interaction.

~M.K. Radhakrishnan, Editor

EDS MEETINGS CALENDAR

(As of 1 December 2014)



THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE:

[HTTP://EDS.IEEE.ORG](http://eds.ieee.org). PLEASE VISIT.

2015 16th International Symposium on Quality Electronic Design (ISQED)	02 Mar - 04 Mar 2015	Santa Clara Convention Center 5001 Great America Pkwy Santa Clara, CA, USA
2015 China Semiconductor Technology International Conference (CSTIC)	15 Mar - 16 Mar 2015	SHICC Shanghai International Convention Center No.2727 Riverside Avenue Pudong, Shanghai, China
2015 IEEE Workshop on Microelectronics and Electron Devices (WMED)	20 Mar - 20 Mar 2015	Student Union Building Boise State University 1910 University Drive Boise, ID, USA
2015 International Conference on Microelectronic Test Structures (ICMTS)	23 Mar - 26 Mar 2015	Doubletree by Hilton Phoenix Tempe 2100 So. Priest Dr. Tempe, AZ, USA
2015 IEEE International Reliability Physics Symposium (IRPS)	19 Apr - 23 Apr 2015	Hyatt Regency Monterey Hotel & Spa 1 Old Golf Course Road Monterey, CA, USA
2015 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)	27 Apr - 29 Apr 2015	The Ambassador Hotel 188 Chung Hwa Road, Section 2 Hsinchu, Taiwan
2015 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)	27 Apr - 29 Apr 2015	The Ambassador Hotel 188 Chung Hwa Road, Section 2 Hsinchu, Taiwan
2015 IEEE International Vacuum Electronics Conference (IVEC)	27 Apr - 29 Apr 2015	Beijing International Convention Center No.8 Beichendong Rd., Chaoyang Dist. 100101, Beijing, China Beijing, China
Abstract submission deadline: 09 Jan 2015 Final submission deadline: 06 Mar 2015 Notification of acceptance date: 09 Feb 2015		

2015 26th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	03 May - 06 May 2015	Hilton 534 Broadway Saratoga Springs, NY, USA
2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)	10 May - 14 May 2015	Kowloon Shangri-La, Hong Kong 64 Mody Road Tsim Sha Tsui East Kowloon Hong Kong
2015 IEEE International Memory Workshop (IMW)	17 May - 20 May 2015	Hyatt Regency Hotel 1 Old Golf Course Road Monterey, CA, USA
2015 International Siberian Conference on Control and Communications (SIBCON) Abstract submission deadline: 24 Mar 2015 Full Paper Submission deadline: 24 Mar 2015 Final submission deadline: 01 May 2015 Notification of acceptance date: 10 Apr 2015	21 May - 23 May 2015	Omsk State Technical University Mira Ave., 11 Omsk, Russia
2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)	01 Jun - 03 Jun 2015	TBD Singapore, Singapore
2015 IEEE 42nd Photovoltaic Specialists Conference (PVSC) Abstract submission deadline: 23 Jan 2015	14 Jun - 19 Jun 2015	Hyatt Regency New Orleans 601 Loyola Avenue New Orleans, LA, USA
2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	05 Oct - 08 Oct 2015	DoubleTree by Hilton Sonoma Wine Country One DoubleTree Drive Rohnert Park, CA, USA
2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) Abstract submission deadline: 01 May 2015 Final submission deadline: 17 Jul 2015 Notification of acceptance date: 29 May 2015	11 Oct - 14 Oct 2015	Sheraton New Orleans Hotel 500 Canal Street New Orleans, LA, USA
2015 IEEE 46th Semiconductor Interface Specialists Conference (SISC)	02 Dec - 05 Dec 2015	the Key Bridge Marriott 1401 Lee Highway Arlington, VA, USA

2015 IEEE International Electron Devices Meeting (IEDM)

Abstract submission deadline: 26 Jun 2015
Final submission deadline: 22 Sep 2015
Notification of acceptance date: 14 Aug 2015

07 Dec - 09
Dec 2015

Hilton Washington
Washington, DC, USA

2016 IEEE International Vacuum Electronics Conference (IVEC)

26 Apr - 28
Apr 2016

Monterey Marriott
350 Calle Principal
Monterey, CA, USA

2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)

05 Jun - 10
Jun 2016

Oregon Convention Center
77 NE Martin Luther King Jr.
Blvd.
Portland, OR, USA

2014 EDS BoG MEETING RECAP AND MAJOR INITIATIVES APPROVED

(continued from page 40)

Secretary's Report & Educational Activities

4. To approve the May 2014 BoG meeting minutes. **Approved**

Constitution and Bylaws

5. To approve the outlined Constitution and Bylaws changes. **Approved**

Publications

6. For 2016, move from financial co-sponsorship to technical co-sponsorship for the Journal of Display Technology (J-DT). **Approved**

Awards

7. To add the Robert Bosch Micro and Nano Electro Mechanical Systems Award to the EDS Awards Committee Charter, which includes adding the Bosch Award as one of the awards that the EDS committee oversees, and adding the Bosch Award Chair to the EDS Awards Committee. **Approved**

Newsletter

8. To approve free online Newsletter access for non-members. **Approved**

Regions & Chapters

9. To approve a new award to add one society level Chapter of the Year Award based on the winners of the regional Chapter of the Year awardees. **Failed**

Technical Committees, Meetings & Fellow Evaluations

10. To approve the list of 2016 repeat conferences. **Approved**

Christopher Jannuzzi
EDS Executive Director

2014 EDS BoG Meeting Recap and Major Initiatives Approved

The EDS Board of Governors (BoG) meeting series was held in conjunction with the 2014 IEEE International Electron Devices Meeting (IEDM) in San Francisco, California, with over a dozen committee and ancillary meetings taking place during the weekend of December 12–14.

Of course, the most important event of the December BoG meeting is the annual elections. This year EDS held a pilot program to have one of the eight BoG Member-at-Large seats elected via the entire EDS membership. There were 1,374 members that voted or 14% of the EDS membership that returned ballots, and they voted to elect Patrick Fay, University of Notre Dame. On December 14, 2014, the EDS Board of Governors (BoG) held its annual election of Members-at-Large for the remaining seven seats.

On behalf of Paul Yu, EDS Nominations and Elections Chair, I am pleased to announce the following are the results of the election:

Members at Large for 2015-2017: Zepnep Celik-Butler*, Steve Chung*, Mukta Farooq, Patrick Fay**, Carmen Lilley, Durga Misra, Hisayo S. Momose, Tian-Ling Ren*

**Individual re-elected for a 2nd term*

***General election winner*

Look for more information on the newly elected members in the next issue of the EDS Newsletter.

In addition to the elections, the following motions were presented to the BoG and voted on:

President's Report

1. To approve the proposed list of 2015 appointments. **Approved**
2. To approve the Asian Flagship Conference AdHoc Committee. **Approved**

Treasurer's Report

3. To approve the 2015 budget. **Approved**

(continued on page 39)